REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

In the present Office Action, Claims 12-28 stand rejected under 35 U.S.C. §112, first paragraph, as allegedly containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In particular, Claims 12 and 28 recite that the interconnect is located between the p-type gate portion and the n-type gate portion. Additionally, Claim 13 is rejected as not having enablement for the feature of "said p-type portion, said n-type portion, said interconnect portion, said planarizing structure having a lateral dimension that is substantially the same."

In response to the above rejections, applicants have amended Claims 12 and 28 to positively recite that the interconnect is *located at least over* the p-type gate portion and the n-type gate portion. Support for this amendment to Claims 12 and 28 is found at Page 8, lines 1-3 as well as in FIGS. 4A-4B.

In addition to the above amendment to Claims 12 and 28, applicants have also amended Claims 12 and 28 to include more structural features of the invention described and illustrated in the present application. In particular, applicants have amended Claims 12 and 28 to positively recite the presence of *a patterned stack which includes at least a vertical semiconductor body having exposed sidewalls located on an upper surface of a substrate*. Support for this amendment to Claims 12 and 28 is found at Page 5, lines 18-21 and in FIGS. 1A-1B.

Claims 12 and 28 have also been amended to positively recite the presence of *a gate dielectric located on each exposed sidewall of the vertical semiconductor body*. Support for this amendment to Claims 12 and 28 is found at Page 6, lines 26-28 as well as FIGS. 2A-2B. Moreover, Claims 12 and 28 have been amended to positively recite that the p-type gate portion *is located on one side of the vertical semiconductor body* and the n-type portion *is located on an opposing side of the* vertical semiconductor body. Support for this amendment to Claims 12 and 28 is found at Page 7, lines 16-20, as well as FIGS. 3A-3B.

Claims 12 and 28 have also been amended to positively recite that the gate portions are located on the upper surface of the substrate and are separated from the vertical semiconductor body by the gate dielectric. Support for this amendment to Claims 12 and 28 is found in FIGS. 3A-3B of the present application as well as at Page 7, lines 16-20.

In addition to amending Claims 12 and 28, applicants have also amended Claim 13 to positively recite that the p-type gate portion, the n-type gate portion, the interconnect, and the planarizing structure have substantially the same final shape. Support for the amendment to Claim 13 is found at Page 9, lines 9-11 of the instant application.

Other amendments to the claims include cancellation of Claim 19 and a minor amendment to Claim 23.

Since the above amendments to the claims do not introduce any new matter into the instant application, entry thereof is respectfully requested. Moreover, the amendments made to Claims 12, 13 and 28 obviate the §112, first paragraph rejection

raised in the present Office Action; therefore applicants respectfully request reconsideration and withdrawal of the formal ground of rejection.

Claims 12 and 19-27 stand rejected under 35 U.S.C. §102(e) as allegedly anticipated by U.S. Patent No. 6,503,784 to Enders, et al. ("Enders, et al."). Claims 14-18 and 28 stand rejected under 35 U.S.C. §103 as allegedly unpatentable over the disclosure of Enders, et al.

With respect to the §102(e) rejection, it is axiomatic that anticipation under §102 requires that the prior art reference disclose each and every element of the claim to which it is applied. In re King, 801 F.2d 1324, 1326, 231 U.S.P.Q. 136, 138 (Fed. Cir. 1986). Thus, there must be no differences between the subject matter of the claim and the disclosure of the applied prior art reference. Stated another way, the reference must contain within its four corners adequate direction to practice the invention as claimed. The corollary of the rule is equally applicable: The absence from the applied reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 1571, 230 U.S.P.Q. 81, 84 (Fed. Cir. 1986).

Applicants respectfully submit that Claims 12 and 19-27 of the present application are not anticipated by the disclosure of Enders, et al. since the applied reference does not teach applicants' claimed structure recited in amended Claim 12. Specifically, Enders, et al. do not disclose an asymmetric FET which includes, among other features, *a patterned stack including at least a vertical semiconductor body having exposed sidewalls located on an upper surface of a substrate*; *a gate dielectric located on each exposed sidewall of said vertical semiconductor body*; and *a p-type gate portion located on one side of the vertical semiconductor body and an n-type portion located on*

an opposing side of the vertical semiconductor body, said gate portions are located on said upper surface of the substrate and are separated from the vertical semiconductor body by said gate dielectric.

In Enders, et al., the transistors are formed **into trenches** that are located below an upper surface of a semiconductor body. The trench sidewalls are lined with a gate dielectric material and then filled with a gate conductor. As such, Enders, et al. do not disclose applicants' claimed asymmetric FET that includes *a patterned stack including at least a vertical semiconductor body having exposed sidewalls located on an upper surface of a substrate*. Moreover, since the gate conductor is formed into the trenches that lay beneath the upper surface, Enders, et al. do not disclose a structure in which the gate portions are on an upper surface of the substrate.

The foregoing remarks clearly indicate that the applied reference does not teach each and every aspect of the claimed invention as required by King and Kloster Speedsteel; therefore the claims of the present application are not anticipated by the disclosure of Enders, et al.

Turning to the various §103 rejection, applicants respectfully submit that the claims of the present application are not made obvious from the disclosure of Enders, et al. since the applied reference does not teach or suggest applicants' asymmetric FET. Specifically, Enders, et al. are defective for the various reasons mentioned above. To reiterate: Enders, et al. do not teach or suggest applicants' claimed structure recited in amended Claim 12 or amended Claim 28. Specifically, Enders, et al. do not teach or suggest an asymmetric FET which includes, among other features, *a patterned stack including at least a vertical semiconductor body having exposed sidewalls located on an*

upper surface of a substrate; *a gate dielectric located on each exposed sidewall of said vertical semiconductor body*; and *a p-type gate portion located on* one *side of the vertical semiconductor body and an n-type portion located on an opposing side of the vertical semiconductor body, said gate portions are located on said upper surface of the substrate and are separated from the vertical semiconductor body by said gate dielectric.* In contrast, Enders, et al. disclose that the transistors are formed **into trenches** that are located below an upper surface of a semiconductor body. The trench sidewalls are lined with a gate dielectric material and then filled with a gate conductor. As such, Enders, et al. do not teach or suggest applicants' claimed asymmetric FET that includes *a patterned stack including at least a vertical semiconductor body having exposed sidewalls located on an upper surface of a substrate*. Moreover, since the gate conductor is formed into the trenches that lay beneath the upper surface, Enders, et al. do not teach or suggest a structure in which the gate portions are on an upper surface of the substrate.

The §103 rejection also fails because there is no motivation in the prior art reference that suggests modifying the prior art structures to arrive at applicants' claimed asymmetric FET which includes the various features recited in amended Claims 12 and 28. The §103 rejection is thus improper since the prior art does not suggest this drastic modification, which is required in the claims of the present application.

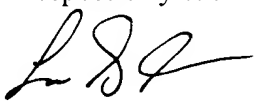
The law requires that the prior art reference provide some teaching, suggestion or motivation to make the modification. Here, there is no motivation provided in the disclosure of Enders, et al. which would lead one skilled in the art to form the transistors on an upper surface of the substrate. Instead, Enders, et al. require that the transistors be formed into trenches that are etched into the substrate. "The mere fact that

the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Fritch, 972 F.2d 1260, 1266, 23 U.S.P.Q. F.2d 1780, 1783-84 (Fed. Cir. 1992). There is no suggestion in the prior art to modify the semiconductor structures to one having applicant's claimed features. As such, the claims of the instant application are not obvious from the disclosure of Enders, et al.

Based on the above amendments and remarks, the rejection to the claims under 35 U.S.C. §103 has been obviated; therefore reconsideration and withdrawal of the instant rejections are respectfully requested.

Wherefore, reconsideration and allowance of the claims of the present application, as amended herein, are respectfully requested.

Respectfully submitted,



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